Low Level RF Control System for SSRF

WANG Fang[1;1)]   WANG Guang-Wei[2]   LU Jian-Fa[1]

1(Shanghai Institute of Nuclear Research, CAS, Shanghai 201800, China)

2(Institute of High Energy Physics, CAS, Beijing 100039, China)

Abstract   The low level RF control system is an essential part of the RF system for Shanghai Synchrotron Radiation Facility (SSRF). In the R&D of the SSRF, one set of low level control system was developed. It consists of a 500MHz signal generator, three feedback loops, an interlock and a protection system. This paper addresses the design of this system and mainly introduces the three feedback loops.

Key words   low-level, feedback control, phase, amplitude, frequency, stability

1   Introduction

In the current RF system design, 8 normal conducting RF cavities are used to provide 4MV RF voltage to the beam. Each cavity will be powered by a 180kW klystron power amplifier and controlled by a low level RF system. The related parameters of the storage ring are shown in Table 1.

Table 1.   Storage ring parameters related to RF system.

Beam energy	E	3.5	GeV
RF frequency	f_{rf}	499.65	MHz
Harmonic number	h	660	
RF voltage	V	4.0	MV
Beam current	I	300	mA
Energy loos/turn	U_0	1256	keV
Synchrotron frequency	f_s	6.9	kHz
Natural bunch length	σ_ℓ	4.6	mm

In the R&D of the SSRF, a high power RF system has been established, which contains a klystron and its power supply from THALES and THOMCAST, a circulator from AFT, a copper cavity borrowed from the PF, KEK, and low level RF control loops developed at the SSRC.

The low level RF system consists of three feedback loops, a signal generator, an interlock and a protection system. The design is basically similar to those of many other electron storage rings in the world, and is based on the use of conventional, and well-proven equipments.

2   Feedback loops

In the RF control system, the reference RF signal is generated by a master oscillator(HP4437B), which is located at the central control room. This system is comprised of three loops and an interlock system. The frequency loop keeps each cavity in a precision, which can be set to 150Hz[1]. The amplitude loop keeps the cavity gap voltage stable within 1%, which acts on the driving power of the plant. And the phase loop keeps the phase stability of the output power of the RF plant within 1 degree at any power level. The interlock system is comprised of a fast vacuum protection, an RF switch and an arc detector. It can ensure the high power RF system the work safely. The schematic diagram of the low level RF control system is shown in Fig.1.
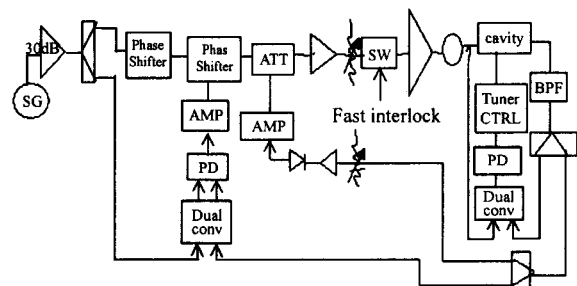

Fig.1.   Block diagram of low level control RF system.

2.1 Tuning loop

The tuner is driven by an AC motor, to compensate the thermal detaining and react the beam loading. The tuning scheme is as follows. First, make the loop open and search the tuner position of the minimum power reflection by moving the tuner manually, since when the beam is absent, the tuner condition of the cavity corresponds to the minimum reflection. Secondly, adjust the output of the phase detector[2,3] to zero by adjusting the machine phase shifter to the minimum reflection tuner position. And at last, close the loop for the actual operation. The loop measures the phase between the cavity voltage and the input RF voltage, which drives the motor to move the tuner. The bandwidth of this loop is around 1 Hz. The maximum tuning speed is 1kHz/s. All of these requirements are essential for the entire accelerator RF system. Also known as, the individual RF system needs tighter control margin than that. In fact, this machine operates at 3 degrees phase offset. The cavity tuning is performed by a deformation of the cavity in the direction of its axial length. The frequency loop controls the AC motor, which drives the tuning cage. The tuning signal is offered by a 1MHz phase detector. The range of the tuner is 92mm. The sensitivity of tuning frequency of the tuning plug is about 50kHz/mm. The nominal speed is 1kHz/s. Actually, the speed can be set by the PLC, and the speed is only limited by the motor and the driver. In the test, we tried to change the frequency of the cavity through changing the environment temperature or just sticking something into the cavity. The result of the test is shown in Table 2.

Table 2. Low level performance.

Loop	Design performance			Test performance		
	Resolution	Dynamic range	Dynamic response	Resolution	Dynamic range	Dynamic response
F-loop	~ 150Hz (adjustable)	± 30°	Tuning speed > 1kHz/s	~ 150Hz (adjustable)	± 30°	Tuning speed > 1kHz/s
A-loop	1 %	Phase ± 30° Power 10dB	Recovery time (20 % step) < 10ms	1 %	Phase ± 30° Power 10dB	Recovery time(100 %) < 1ms
P-loop	± 1°		Recovery time (20 % step) < 10ms	± 1°	< 0.5°	Recovery time (± 30°) < 1ms

2.2 Amplitude loop

RF signals picked up from the end of the cavity, which belongs to one control unit, are sent via phase stable coaxial cable to the control loops. The measured data of relative phase of these RF signals show that the deviations are small. The signals can be adjusted at the RF combiner using attenuators, whose attenuation accuracy is 0.1dB, and a machine phase shifter, whose accuracy is ± 1°[1]. The amplitude loop keeps the gap voltage constant by measuring the magnitude of the cavity field, comparing it to a reference voltage, and adjusting the electronic control attenuator in the main signal circuit. In the complicated condition, the power dissipated on the cavity surface will have to remain constant. The result of the test is listed in Table 2. The bandwidth of this loop is also of the order of 1 kHz[2]. The RF amplitude linear detector works within an error ± 1 % over a range of 35dB, from the maximum 20dBm down to-15dBm. The gain of this feedback loop is between 20dB and 40dB, depending on the RF output level as mentioned in the previous section.

2.3 Phase loop

This loop is to keep the phase of the fields in the cavities locked with the master signal generator. And in fact there is an error of phase shifter. The control precision should be less than ± 1°. The phase loop will also compensate the phase change with the RF power variance, due to the power amplifier, the circulator, the klystron, the driving electronics and so on. The components of the driving electronics are designed to have a small phase variation over a wide operating range. The Phase Detector (PD), which convert the signal from 499.65MHz to 1MHz, is the key component. The sensitivity of the PD is 50mV/degree. The range of the detector is ± 180°. The PD is a device with rather constant sensitivity against

large power variations. The phase detection system works within on error of $\pm 1°$ for the input power level between 0dBm and -35dBm. This will prevent the effect of amplitude modulations on the operation of the loop.

Although the low level control RF system is designed to work with a closed loop mode, the operation with open loop is also tested. This is useful during the final commissioning period. Now we have completed the bench test for every loop individually, and the last acceptance test has been done too.

All the components of the system, including the cables, connectors and so on, are completely tested to certify the specifications. For each plant, the low-level system is hosted in three racks. Two of these racks contain the frequency loop, and the phase loop. The third rack contains the remaining component of the low level RF control system. The system will be built in a modular way, which eases installation, maintenance and operation.

3 Interlock system

This system is required to turn off the RF driver and high voltage power supply in the event of arcing in the cavity windows, the klystron window, or the circulator, which are very essential and expensive. Infrared photodiodes receive arc signals through radiation resistant optical fibre. A PLC implements the basic control function. A PC computer communicates with the PLC by a an RS-232 port, and it also connects the local network. Various sensors and gauges are installed to neasure the following factors: the temperature (cooling water, cavities, windows, circulators, water load, tuners), the pressure and flow (cooling water and air), the position of tuners, and connected with the I/O unit of PLC. The fast interlock runs in parallel and shuts down the system when a major fault occurs, independent on each other.

4 Fast protection

4.1 Arc detection

A 10m long fibre optic cable brings the arc detection light to the fast Interlock module. The detector is a Hon-

eywell HFD-3854 PIN photodiode with a peak response wavelength of 850nm. Each channel has both adjustable gain and bandwidth setting jumpers. The fastest response time is about $1\mu s$ and the slowest can be up to $10\mu s$. Slower settings enable controlled timing of the trip. The photodiode output is amplified in two stages to achieve a gain of about 135dB. Each channel has slow DC removal ($>$1ms) to allow the use of high gain without regarding to the offsets that would normally restrict such a gain. Only fast transient light events are triggered. The unbiased response time of the photodiode is fast enough that no reverse biasing is required. The resulting speed increase from reverse biasing would be small compared to the overall response time anyway, and dark current noise would increase. The noise equivalent power is approximately $0.05\mu W$. The preamp output is buffered and available at the front panel of the external chassis for testing and monitoring purposes.

4.2 Fast vacuum protection

Fast protection is very important for system's safety at high power. Some high power components are expensive and sensitive, such as ceramic window, circulator and klystron. When some parameters of the system states (cavity voltage, forward power, reflection power, vacuum, etc.) exceed threshold or major failure occurs, it switches off the drive signal in prevent breakdown of components or paralysis of system. Arc Detectors for ceramic window fast Vacuum detector preventing 2—7ms speed are also included in this part.

5 Conclusion

The result of high power test is as follows: the performance of the low level system is good in the range of 185—420kV. When these three loops operate for more than 8 hours at one time the stability of phase is $< \pm 1°$ and the stability of amplitude is 1 %, the result of the test is shown in Fig.2.

The peak power in the cavity is greater than 20kW and the peak input power is greater than 25kW. We foresee to get a better operating condition of the control system when the three control loops and the interlock system are commissioned as a whole in the extensive test on the cavi-
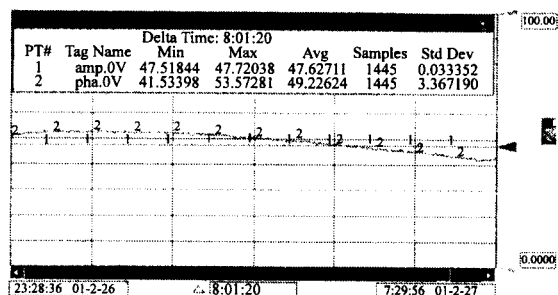
Fig.2. The test of 8hr phase and amplitude stability.

ty. The problem on how to ensure the whole system, including three low level control loops, to work stably at a high beam current, will be researched and solved in the near future. The 50Hz noise caused by the power supply and AC interference of harmonics will directly influence the control precision of the loops. So, independent power supply system is adopted for the low level RF system to avoid the common line with magnet power supply, injector system and control system. One point ground and good shield are adopted in the system, and the interference between the stages and loops are avoided.

Explain:Phase:50mV/(°),

phase stability:$(53.572 - 41.533)(\mathrm{mV})/50(\mathrm{mV})$
$= 0.24(°)$,

amplitude stability:$\dfrac{(47.720 - 47.518)/2(\mathrm{mV})}{(47.720 + 47.518)/2(\mathrm{mV})} =$
0.2%.

References

1　Fabrisetal A. Characterisation of the Low Level System of the ELETTRA RF Plants, EPAC96 Sitges, 1996

2　KEK B-Factory Design Report, KEK Report 95

3　Hara M et al. RF Stations of the Spring-8 Storage Ring, Proceedings of the PAC97 Meeting of the American Physical Society. Vancouver, Canada, 1997

SSRF 高频低电平系统

王芳[1;1)]　　王光伟[2]　　陆建法[1]

1 (中国科学院上海原子核研究所　上海　201800)

2 (中国科学院高能物理研究所　北京　100039)

摘要　整个高频系统包括谐振加速腔、高频功率源和 180kW 发射机、低电平控制与连锁保护. 高频工作频率为 499.65MHz. SSRF 500MHz 低电平控制系统由信号源、反馈控制回路 (频率调谐环路、相位控制环路、幅度控制环路) 和连锁保护等构成. 加速器高频腔控制系统的稳定性是加速器设计中一项重要指标, 特别是在高流强条件下, 更是对高频的稳定性提出了较高的要求. 如何在加速器中合理地利用先进技术, 是整机工作在稳定可靠而又易于控制的状态是低电平系统分析与设计的任务. 由于高频系统庞大, 低电平控制的对象复杂, 作为加速器高频系统中的控制, 无论其基础理论还是电子线路, 在其各自的领域中都属于比较成熟的东西, 但将他们结合起来, 组成一个系统并要求系统性能最优, 也有一些特殊的难度和要求. 例如强束流与加速腔之间的耦合, 用腔到束流的传递函数来描述, 都是其他系统控制领域中所没有的问题, 又要考虑几百千瓦的微波功率器件, 它们之间还存在着复杂的耦合, 这都增加了系统设计的难度. 同时各种回路组成系统时, 随机产生的干扰信号也是必须考虑的因素. SSRF 系统对低电平控制的要求:1) 使各腔间电压相位一致;2) 使总加速电压和幅度稳定;3) 使腔的频率正确调谐;4) 发生异常状态时, 保证设备的安全连锁. 本文介绍了这个系统的构成和原理、技术指标、安装调试和测试结果.

关键词　低电平　反馈控制　相位　幅度　频率　稳定性