Research on total-dose hardening for H-gate PD NMOSFET/SIMOX by ion implanting into buried oxide

QIAN Cong(钱聪)[1] ZHANG Zheng-Xuan(张正选) ZHANG Feng(张峰) LIN Cheng-Lu(林成鲁)

(Shanghai Institute of Microsystems and Information Technology, CAS, Shanghai 200050, China)

Abstract In this work, we investigate the back-gate I-V characteristics for two kinds of NMOSFET/ SIMOX transistors with H gate structure fabricated on two different SOI wafers. A transistors are made on the wafer implanted with Si^+ and then annealed in N_2, and B transistors are made on the wafer without implantation and annealing. It is demonstrated experimentally that A transistors have much less back-gate threshold voltage shift ΔV_{th} than B transistors under X-ray total dose irradiation. Subthreshold charge separation technique is employed to estimate the build-up of oxide charge and interface traps during irradiation, showing that the reduced ΔV_{th} for A transistors is mainly due to its less build-up of oxide charge than B transistors. Photo-luminescence (PL) research indicates that Si implantation results in the formation of silicon nanocrystalline (nanocluster) whose size increases with the implant dose. This structure can trap electrons to compensate the positive charge build-up in the buried oxide during irradiation, and thus reduce the threshold voltage negative shift.

Key words silicon on insulator, total-dose irradiation effect, H gate, subthreshold charge separation, photo-luminescence

PACS 78.55.Ap, 73.22.-f, 81.05.Cy

1 Introduction

Silicon-on-insulator (SOI) technology offers some hardness advantages over the bulk-silicon technology for space and other applications. For example, properly designed SOI circuits are less prone to single-event upset from energetic cosmic particles than the equivalent bulk-silicon intergrated circuits. However, the positive charge build-up in buried oxide (BOX) makes hardening SOI devices for use in the total dose radiation environments (e.g., space) much more challenging than for the bulk-Si devices[1, 2]. Large concentrations of oxides-trapped charge cause large negative threshold-voltage shift, and even result in device failure by shifting the operating voltage. Positive charge trapping in the buried oxide can invert the back-channel interface of partially-depleted n-channel transistors, and form a conductive channel between the source and the drain. This can lead to large increase in leakage current in intergrated circuits using partially-depleted transistors.

Ion implantation has been proved to be an effective way to prepare radiation-hard materials. There has been considerable research on hardening the SIMOX materials in recent years, and developing a variety of hardening techniques such as multiple oxygen implantation followed by multiple annealing after each implantation, supplemental oxygen implantation, internal thermal oxidation, fluorine ion implantation, nitrogen ion implantation, nitrogen-Oxygen co-implantation, etc. Recently, silicon ion implantation has been a novel method to harden the buried oxides of SIMOX. A number of studies[3, 4] has been done to research the irradiation properties and its mechanism of silicon-implanted SIMOX and transistors fabricated on it.

We have studied the X-ray total-dose irradiation effect of hardened partially-depleted NMOS transistor with H gate fabricated on silicon-implanted SIMOX. We have also demonstrated by PL research that the implantation-induced Si nanocrystals in the oxide can restrain the positive charge buildup in the

Received 26 March 2007

1) E-mail: qiancong@263.net

buried oxide during irradiation so as to enhance its radiation hardness.

2 Experiment

The studied NMOS/SOI transistors are fabricated on SIMOX wafers with 200 nm thick top silicon and 380 nm thick BOX, which is appropriate for the scaled deep submicron devices. One wafer is hardened by implanting with silicon at an dose of $1\times10^{15}/\mathrm{cm}^2$ (the implantation peak is located at 100 nm below the top gate-BOX interface) and then annealed at 900 ℃ in N_2 ambience for 0.5 h. The other wafer is not implanted (control sample). The MOSFETs fabricated on the implanted wafer and control wafer are labeled A and B, respectively. A and B MOSFETs have the same fabrication technique.

H gates (Fig. 1(a)) are employed in both A and B MOSFETs. Transistors with H gate design can be used in radiation environments to prevent the kink or bipolar effect since the body contacts are present at both ends of the channel[5]. Furthmore, the H gate structure offers no direct edge leakage path between the source and the drain (the edges run only from N^+ to P^+ diffusions)[5]. The body is grounded to eliminate the floating body effect. The gate oxide thickness is 41 nm, the gate length is 3 μm and the aspect ratio W/L is 60∶3. LOCOS (Local Oxidation of Silicon) is used to enforce the trench and prevents any interaction of the gate bias on the buried oxides. The use of external body contact suppresses the floating-body effect and bipolar effect, avoids the appearance of lateral leakage current induced by trapping in isolation oxides and LOCOS, and prevents the drain-source breakdown.

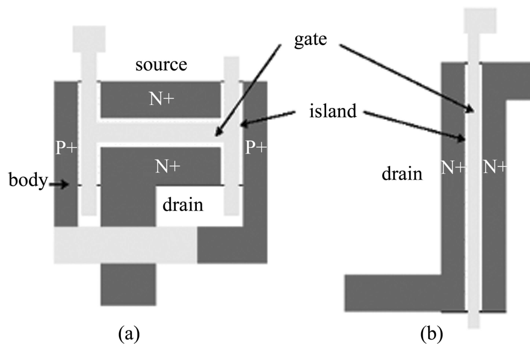

Fig. 1. The schematic diagram of two gate structures. (a) H gate; (b) Regular gate.

Figure 2 shows the equivalent circuit of an SOI NMOS transistor[6] . It consists of a main front channel transistor with top gate, a bipolar transistor with the body being the base (floating or grounded, in our work, it's grounded), and a back channel transistor with back-gate. The bipolar transistor is rarely turned on operation at 5 V for a 3 μm transistor so that the front channel and back channel transistor can be evaluated independently in the partially-depleted SOI transistor structure when V_{DD}=5 V.

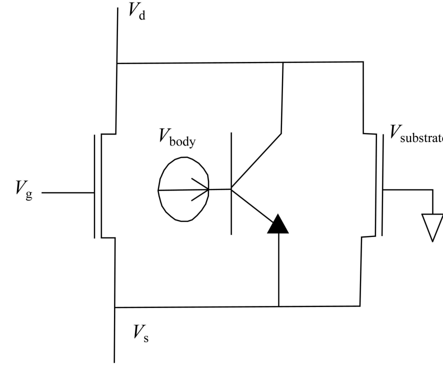

Fig. 2. The equivalent circuit of an SOI NMOSFET (V_{body}=0 V).

Transistors are irradiated with 10 keV X-rays generated by the ARACOR 4100 Automatic Semiconductor Irradiation System at a dose rate of 27 krad (SiO_2)/min. Three bias conditions during irradiation are given in Table 1, they are on-state, off-state and pass-gate (transmission-gate). Pre-radiation and Post-radiation (at a series of doses) I-V characteristics of back channel transistors were measured by the HP 4155 Semiconductor Parameter Analyzer. The total dose radiation effect was characterized by the radiation-induced threshold voltage shifts as a function of the total dose up to 2.7 Mrad (SiO_2). Each transistor was measured within 10 min after being subjected to X-ray irradiation.

Table 1. Bias conditions during the total-dose irradiation, V_{DD}=5V.

	source/V	drain/V	gate/V	body/V	substrate/V
ON	0	0	V_{DD}	0	0
OFF	0	V_{DD}	0	0	0
PG	V_{DD}	V_{DD}	0	0	0

3 Results and discussion

3.1 Results of irradiation experiment

Figure 3(a) shows the threshold voltage shifts of the back-gate transistor under three different biases during irradiation at 90 krad, 180 krad, 540 krad, 900 krad, 1.8 Mrad and 2.7 Mrad (SiO_2), which were extracted from the back-gate I_{d}-V_{g} characteristics at a drain current $I_{\mathrm{d}}=10^{-6}$A. Obviously, A transistors have less bake-gate threshold voltage shifts than B transistors at any irradiation dose and under all bias conditions, indicating that Si implantation restrains the negative shift of back-gate threshold voltage. PG is the worst bias state for B transistors while OFF is the worst bias state for A transistors.

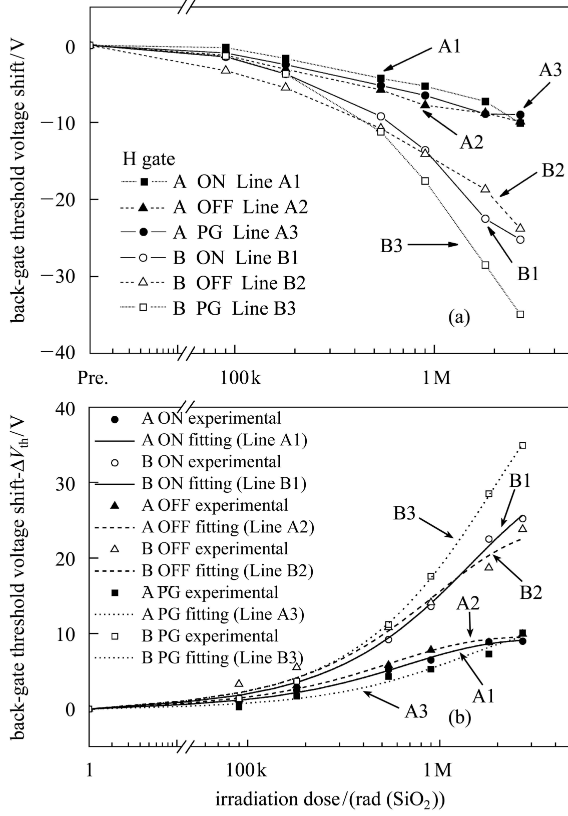

Fig. 3. Back-gate threshold voltage shift as a function of the total dose for NMOSFET/ SIMOX. (a) experimental; (b) fitting.

Table 2 demonstrates the ($\Delta V_{\rm th}$(A)$-\Delta V_{\rm th}$(B)) value as the function of irradiation dose, with $\Delta V_{\rm th}$(A) representing the back-gate threshold shift of an A transistor and $\Delta V_{\rm th}$(B) representing the back-gate threshold shift of a B transistor. The ($\Delta V_{\rm th}$(A)$-\Delta V_{\rm th}$(B)) value of PG bias is the largest one when the irradiation dose is above 540 krad (SiO_2). It indicates that silicon implantation can effectively harden the SOI on which A transistors are fabricated, under all three biases, thus preventing them from failure induced by the threshold voltage shift of the back-gate transistor.

The curves in Fig. 3(a) have been fitted to a recently proposed model[6] describing the back n-channel threshold voltage shift induced by radiation:

$$\Delta V_{\rm th}=-\frac{qN_{\rm ot}}{\kappa\varepsilon_0}t_{\rm BOX}\left[1-\exp\left(-\alpha t_{\rm BOX}\frac{\rho D}{\omega N_{\rm ot}}\right)\right], \quad (1)$$

where D is the total dose in rad (100 erg/g), ρ/ω (=7.6×10^{12} pairs/rad) is the excited electron-hole pairs per unit radiation, κ (=3.9) is the dielectric constant, ε_0 (=8.85×10^{-14} f/cm^{-2}) is the permittivity of vacuum, $t_{\rm BOX}$ is the buried oxide thickness (in this paper, $t_{\rm BOX}$= 380 nm), $N_{\rm ot}$ is a saturated net positive charge density, and α is the fraction of hole capture. Note that the value of $N_{\rm ot}$ depends on the irradiation bias. The fitting curves are given in Fig. 3(b).

The values of $N_{\rm ot}$ and α calculated by Origin 7.0 during the fitting are given in Table 3 below. It is clearly demonstrated that A transistors have smaller saturated net positive charge density $N_{\rm ot}$ and the fraction of hole capture α than B transistors under all three bias conditions. The reductions of $N_{\rm ot}$ and α values are definitely attributed to silicon implantation to the BOX and the following annealing. Moreover, PG bias has the largest $N_{\rm ot}$ while OFF bias has the largest α, for both A and B transistors.

Table 2. The ($\Delta V_{\rm th}$(A)$-\Delta V_{\rm th}$(B)) value as a function of irradiation dose for H-gate (V).

bias	90 krad(SiO_2)	180 krad(SiO_2)	540 krad(SiO_2)	900 krad(SiO_2)	1.8 Mrad(SiO_2)	2.7 Mrad(SiO_2)
ON	0.45	1.19	3.97	7.07	13.62	16.17
OFF	2	2.4	5	6.3	9.9	13.85
PG	1.1	2	6.9	12.3	21.2	24.8

Table 3. The fitting-calculated $N_{\rm ot}$ and α value.

	ON, A	ON, B	OFF, A	OFF, B	PG, A	PG, B
$N_{\rm ot}$/cm^{-3}	5.27×10^{11}	1.73×10^{12}	5.46×10^{11}	1.36×10^{12}	6.34×10^{11}	2.65×10^{12}
α	2.71×10^{-3}	4.10×10^{-3}	3.41×10^{-3}	4.94×10^{-3}	1.60×10^{-3}	4.74×10^{-3}

3.2 Separating the irradiation-induced shifts of oxide charge and interface traps

Subthreshold-current measurements[7], for splitting an irradiation-induced threshold-voltage shift ($\Delta V_{\rm th}$) into a contribution due to interface traps $\Delta V_{\rm it}$ and a contribution due to trapped-oxide charge $\Delta V_{\rm ot}$ (where $\Delta V_{\rm th}=\Delta V_{\rm it}+\Delta V_{\rm ot}$), are used to determine the increase in the quantity of interface states, $\Delta N_{\rm it}$ (cm^{-2}), and trapped-oxide charge, $\Delta N_{\rm ot}$ (cm^{-2}). If the interface states (interface traps) are neutral when the Fermi level is at the midgap, $\Delta V_{\rm it}$ and $\Delta V_{\rm ot}$ can be estimated by the following equation:

$$\Delta V_{\rm ot}=V_{\rm mg}(\text{post-rad})-V_{\rm mg}(\text{pre-rad}), \quad (2)$$

$$\Delta V_{\rm it}=V_{\rm so}(\text{post-rad})-V_{\rm so}(\text{pre-rad}), \quad (3)$$

where $V_{\rm mg}$ is the midgap voltage and we define the stretch-out voltage $V_{\rm so}=V_{\rm th}-V_{\rm mg}$. Eq. (2) shows that the threshold-voltage shift due to the trapped oxide

charge $\Delta V_{\rm ot}$ equals to the shift of the midgap voltage $V_{\rm mg}$ during the irradiation. Eq. (3) presents that the threshold-voltage shift due to the interface traps $\Delta V_{\rm it}$ equals to the shift of the stretch-out voltage $V_{\rm so}$ during the irradiation. Then the irradiation-induced increase in the quantity of net positive trapped-oxide charge $\Delta N_{\rm ot}$ and interface states $\Delta N_{\rm it}$ are given by Eqs. (4) and (5), respectively:

$$\Delta N_{\rm ot} = -\Delta V_{\rm ot} C_{\rm ox}/q\,, \qquad (4)$$

$$\Delta N_{\rm it} = \Delta V_{\rm it} C_{\rm ox}/q\,, \qquad (5)$$

where $C_{\rm ox}$ is the capacitance of the oxide per unit area, given by $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$, with $t_{\rm ox}$ being the thickness of the gate oxide. The increase of trapped oxide charge (positive) will cause the negative shift of $V_{\rm ot}$, while the increase of interface states (in most cases, they are negative) will result in the positive shift of $V_{\rm it}$.

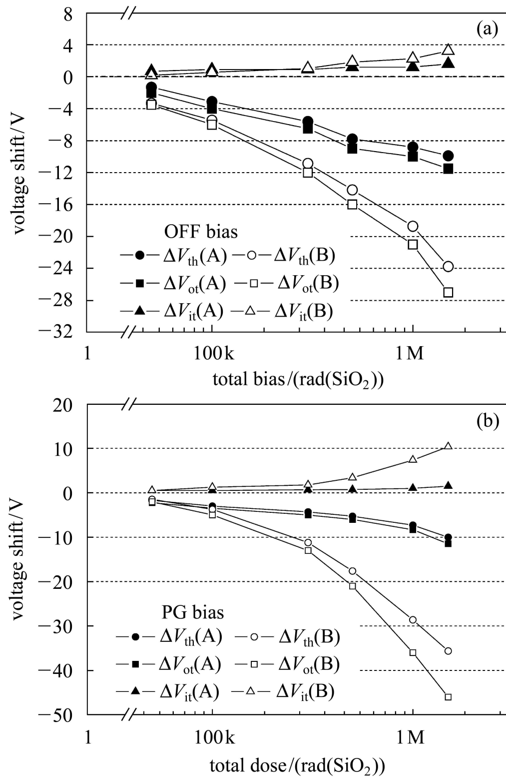

Fig. 4. Back-gate threshold voltage shift $\Delta V_{\rm th}$ and contributions to that shift due to oxide charge $\Delta V_{\rm ot}$ and interface traps $\Delta V_{\rm it}$ as a function of the total dose for NMOSFET/SIMOX.

Figures 4(a) and (b) present the $\Delta V_{\rm ot}$ and $\Delta V_{\rm it}$ as a function of the total dose under OFF and PG bias. It is seen that $\Delta V_{\rm ot}$ is negative and $\Delta V_{\rm it}$ is positive, as the absolute value of $\Delta V_{\rm ot}$ is much larger than that of $\Delta V_{\rm it}$, $\Delta V_{\rm th}$ should be negative. When the irradiation dose increases, $\Delta V_{\rm th}$ becomes more and more negative. It is indicated that under any bias, both the $\Delta V_{\rm ot}$ and $\Delta V_{\rm it}$ of A transistors are less than those of B transistors, so the $\Delta V_{\rm th}$ of A is smaller than that of B. The irradiation-induced shift of trapped-oxide charge and interface traps as a function of the total dose are given in Fig. 5(a) and (b), under OFF and PG bias, respectively. We can find that at any radiation dose, the $\Delta N_{\rm ot}$ and $\Delta N_{\rm it}$ of A transistors are less than those of B transistors, especially for PG bias. For an A transistor, OFF is as worse as PG, while for a B transistor, PG is the worst bias. As seen in Fig. 5, $\Delta N_{\rm ot}$ is about a magnitude larger than $\Delta N_{\rm it}$, so the impact of $\Delta N_{\rm ot}$ on the shift of threshold voltage is much larger than the impact of $\Delta N_{\rm it}$. The advantage of A over B lies in the hardening technique of Si implantation which reduces the build-up of net positive trapped-oxide charges, so as to decrease the negative shift of $\Delta V_{\rm ot}$ and $\Delta V_{\rm th}$.

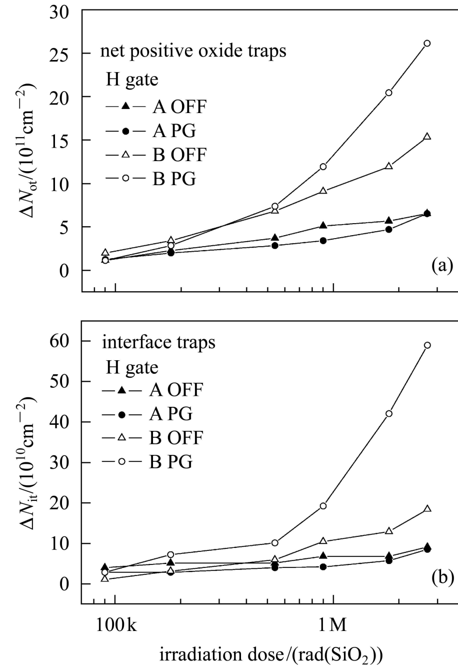

Fig. 5. Effect of the total dose on the build-up of (a) net positive oxide traps and (b) interface traps for A and B transistor.

3.3 Result of photoluminescence

The samples studied were 380 nm thick thermal oxides grown on 10—25 Ω·cm p-type Si (100) substrates at 1000 ℃. According to the TRIM simulation, the Si concentration peak was about 100 nm below the surface of the oxide, which was in accordance with the SOI wafer in previous irradiation research. The implantation doses were 1×10^{14} and 1×10^{15} $\rm Si^+/cm^2$. After implantation, the samples were annealed in N_2 at 900 ℃ for 30 min, the annealing condition was the same as that of SOI wafer. An unimplanted wafer and an Ar implanted wafer were also employed.

Figure 6 (a) shows the room temperature PL spectrum (400—800 nm) from samples implanted with

1×10^{14} and 1×10^{15} Si^+/cm^2 then annealed in N_2 at 900 ℃ for 30 min. The main PL peaks (500—600 nm)

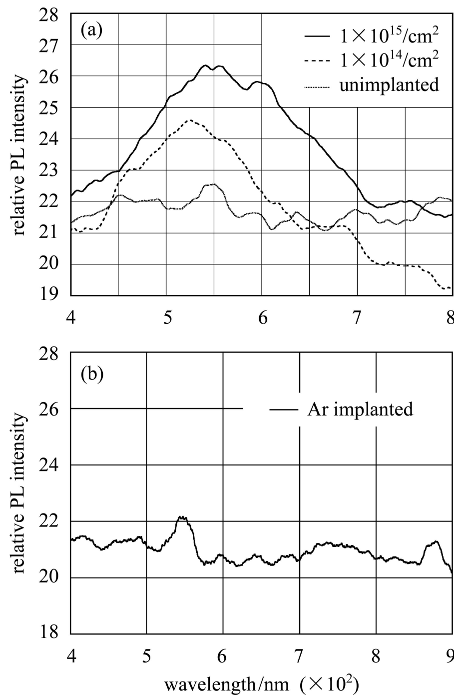

Fig. 6. Photoluminescence intensity as a function of wavelength for oxides implanted with (a) 1×10^{14} or $1\times10^{15}/cm^2$ Si ions, then annealed in Ar for 30 min at 900 ℃, (b) $1\times10^{15}/cm^2$ Ar ions, then annealed in Ar for 30 min at 900 ℃.

are attributed to the emission from silicon nanocrystals which can capture electrons to compensate the build-up of irradiation-induces net positive charge so as to reduce the negative shift of back-gate threshold voltage[8—10]. Note that increasing the implant dose from 1×10^{14} to 1×10^{15} Si^+/cm^2 shifts the PL peak from ~525 to ~575 nm, reflecting the increase of the size of nanocrystals from ~1 nm to ~1.5 nm, as a result of additional agglomeration of implanted Si[11]. No PL peak was observed in either the unimplanted oxide (Fig. 6(a)) or the Ar-implanted sample (Fig. 6(b)). It is suggested that the PL peak is due to implant induced chemical changes rather than the implant induced damages, as Si and Ar implants produce similar amount of damages to the oxide according to SRIM calculations[12]. Si implantation will result in oxidation states Si^{n+} (n= 0, 1, 2, 3, and 4) in the SiO_2 films which can be quantitatively detected by XPS[13], while Ar implant will not cause any chemical change to the oxide as Ar is an inert gas.

4 Conclusion

The back-gate electrical properties of NMOSFET/SIMOX transistors with H gate structure fabricated on SOI wafers are studied in this work. It is experimentally found that A transistors which are fabricated on the wafer implanted with Si^+ have much smaller back-gate subthreshold voltage shifts due to X-ray total dose irradiation than B transistors which are not implanted. Subthreshold charge separation technique is used to split the irradiation-induced threshold-voltage shift (ΔV_{th}) into a contribution due to the interface traps ΔV_{it} and a contribution due to the trapped-oxide charge ΔV_{ot}, and the irradiation-induced build-up of net positive trapped-oxide charges ΔN_{ot} and interface states ΔN_{it} are also estimated. It is indicated that the smaller ΔV_{th} of an A transistor is due to the reduction of ΔN_{ot}. PL emission of thermal oxides which are implanted with Si or Ar and unimplanted are also researched to verify the existence of Si nanocrystals. This structure is due to the chemical change rather than the physical damage caused by the Si implantation. The average size of Si nanocrystals increases with the implantation dose. Si nanocrystals can capture trap electrons to compensate the net positive charge buildup in the buried oxide during irradiation, thus causing the reduction of the ΔV_{th}.

References

1 Schwank J R, Shaneyfelt M R et al. IEEE Transactions of Nuclear Science, 2000, **47**(6): 2175

2 Schwank J R, Fleetwood D M et al. Microelectronic Engineering, 2004, **72**: 362

3 Nicklaw C J, Pagey M P et al. IEEE Transactions of Nuclear Science, 2000, **47**: 2269

4 Mrstik B J, Hughes H L. IEEE Transactions of Nuclear Science, 2003, **50**(6): 1947

5 Jean-Pierre Colinge. Silicon-on-Insulator Technology: Materials to VLSI, 2000. 117

6 LIU S T, Balster S et al. IEEE Transactions of Nuclear Science, 1999, **46**(6): 1817

7 Lenahan P M, Dressendorfer P V. Journal of Applied Physics, 1984, **55**(10): 3495

8 McWhorter P J, Winokur P S. Applied Physics Letters, 1986, **48**(2): 133

9 Ioannou-Sougleridis V et al. Materials Science and Engineering B, 2003, **101**(1—3): 324

10 Photopoulos P, Nassiopoulou A G et al. Applied Physics Letters, 2000, **76**(24): 3588

11 Photopoulos P, Nassiopoulou A G. Applied Physics Letters, 2000, **77**(12): 1816

12 Garrido Fernandez B, Lopez M et al. Journal of Applied Physics, 2002, **91**(2): 798

13 Ziegler J F, Biersack J P. Nuclear Instruments and Methods in Physics Research, 1982, **93**: 194