Design of a very high frame rate camera based on an asynchronous CCD driving method*

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Abstract: A very high frame rate camera is designed based on an innovative CCD driving method. The CCD driving method is mainly implemented on frame transfer CCDs. Asynchronous drive timing sequences are applied in the image and storage section of the CCDs. Several rows of the charge in the image section are binned onto the same row in the storage section, and there are the same number of images to be stored in the storage section before they are read out. Based on the new driving method, the frame transfer CCDs can work at a very high frame rate in acquiring burst images though the reading speed remains at a lower level. A very high frame rate camera is designed in this paper. The innovative CCD driving method is mainly of concern. An e2v's CCD60 is adopted in the camera system, whose full size resolution is 128×128, and the up most frame rate is 1000 Hz in the conventional CCD driving method. By using the presented method, the CCD60 based imager is capable of operating at up to 40000 frames per second (fps) at a recognizable resolution of 128×32. Comparing cameras using traditional binning and region of interest technologies, the frame rate is normally less than 5000 fps while the resolution is only 32×32 left.

Key words: high frame rate cameras, CCD driving, image acquisition

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1 Introduction

High speed cameras based on solid state image sensors have been developed and are widely used in high energy physics and nuclear physics, as well as in many other fields [1–5]. The frame rate is one of the most important specifications in the application of high speed cameras, and cameras requiring a frame rate of more than 10^4 frames per second are mostly needed by researchers [6]. Scientists and engineers have implemented several kinds of method to increase the image acquisition frame rate of the CCD cameras, such as binning [7], region of interest (ROI) and parallel readout. Many of them have been adopted on frame transfer CCDs because of their relatively fast frame rate operation.

A typical frame transfer CCD is divided into three distinct areas (Fig. 1(a)): the image (sensitive) area where images are focused; the storage area where the integrated image is temporarily stored prior to readout; and the serial CCD shift registers. Normally, the storage array is identical in size to the image array and is covered by an opaque mask to shield the pixels from light. After the image array is exposed to light, the entire image is rapidly shifted to the storage array.

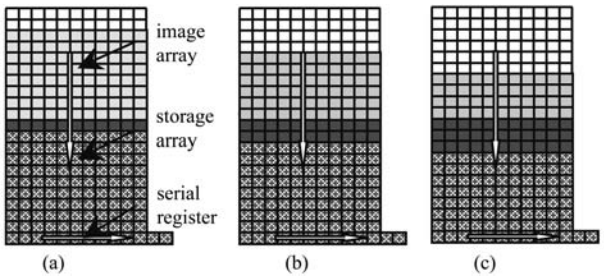

Fig. 1. Principle of the innovative CCD driving method.

In the conventional driving method, the rows in the image array are driven to the storage array row by row, which are then read out serially. While the masked storage array is being read, the image array integrates the charge for the next image. Normally,

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the storage array can only store one image frame before it is read out. Rudolf Germer arranged the sensitive and the storage area of a frame transfer sensor in a different way [8], in which the sensing size is reduced and the shield storage area can be used to keep several image frames. This method provides good resolution in the horizontal direction and limited resolution in the vertical direction. But the view scene area is not standard (rectangle). In some cases, we are interested in getting high frame rate images with a normalized field of view. We arrange a new driving method on frame transfer CCDs, which can achieve a very high repetition rate at a usable resolution as well as a normal field of view.

2 Method

The innovative CCD driving method is shown in Fig 1. In a typical frame transfer CCD driving method, the rows in the image area and the storage area are transferred simultaneously. That is, when a row is transferred to the storage array, there must be a row transferred to the lower section of the storage array. In the altered CCD driving method, the rows are transferred asynchronously in the image and the storage array. Several rows (Fig. 1 shows the two rows as an example) in the image array are transferred onto the row in the storage array. Fig. 1(a) shows that the first two rows (in the lower part near the storage array) are transferred to the first row of the storage array (in the upper part near the image array). After the two rows are transferred to the first row of the storage array, the row in the storage array is transferred to the lower row, and then the next two rows in the image array are transferred to the first row of storage again (Fig. 1(b)), and so on (Fig. 1(c)). After the whole rows in the image array are transferred to the storage array, the image array is ready to make another exposure. In the shown method, there will be two images in the storage array before it is completely filled by the image charges. The main difference between this method and the conventional one is that the image array can be exposed several times before the storage array is read out. Here the storage area can store several image frames of accordingly.

The timing scheme is shown in Fig. 2. A two-phase CCD drive clock is shown by this method but it is not restricted to only the two-phase CCDs. I1, I2 represent the drive clocks in the image area, and S1, S2 represent the drive clock in the storage area. The sensor works in two steps. Step 1 involves the transfer of n lines of pixels in the image array onto the first line of pixels in the storage area continuously, where the charges are binned on the pixels, then transfer one line of pixels in the storage array to the lower line. That is to say, for every n pulses of I clocks, there is an S pulse. n is the number of frames that can be stored in the storage area. Step 2 involves repeating Step until all of the lines in the image area are transferred to the storage area. Now the image array is ready for the next exposure. Step2 is repeated $n-1$ times and the transfer of the image to the storage area is finished. Then the normal serial readout sequence is implemented. Here, the captured image is composed of n frames of image sequence. The resolution of each image is $1/n$ of the normal CCD image. The repeating frame period time includes the frame transfer time and the exposure time.

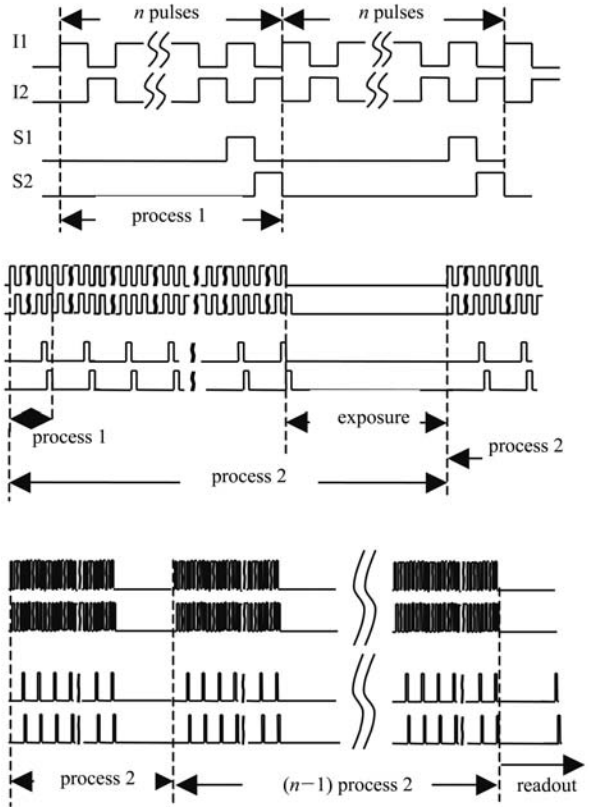


Fig. 2. The innovative CCD timing sequence.

3 The implementation of a very high speed CCD camera

A very high frame rate CCD camera is designed based on the new driving method. The CCD adopted is e2v CCD60 [9], whose full pixel size is 128×128. The device functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and storing sections into the readout register. Following

the transfer through the readout register, the charge is multiplied in the gain register prior to conversion to a voltage by a low noise output amplifier. In this novel output, the device is capable of operating at an equivalent output noise of less than one electron at a frame rate of 1 kHz [10]. Several high frame rate cameras have been developed on CCD60, and these can also work at a high frame rate to several thousands of frames per second [11], combining binning and the region of interests (ROI) readout method.

The camera designed in this paper includes a CCD60 image sensor, a CPLD (XC95108-7C) from Xilinx Inc., which is used to generate the CCD drive timing and the camera logic sequences, a video signal processing circuit (VSP2000) acting as the correlated double sampling and signal amplifying, and a data interface, which is used to encode the digital signal for transferring to the remote area (Fig. 3).

The drive timing sequence is arranged as the new method (Fig. 4). Channel 1 indicates the timing sequence of I (in the image area) and Channel 2 shows the corresponding timing sequence of S (in the storage area). In Fig. 4(a), one storage area row is transferred after every four image area rows are transferred, which achieved 4:1 binning. In Fig. 4(b), four frames of image are transferred before they are read out from the CCD. That is, every four rows of charges in the image area are binned onto one row of the wells in the storage section, and four image frames can be stored in the CCD storage area before they are read out.

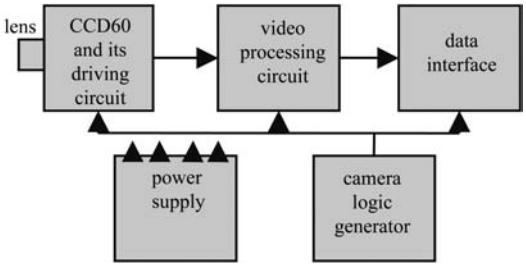
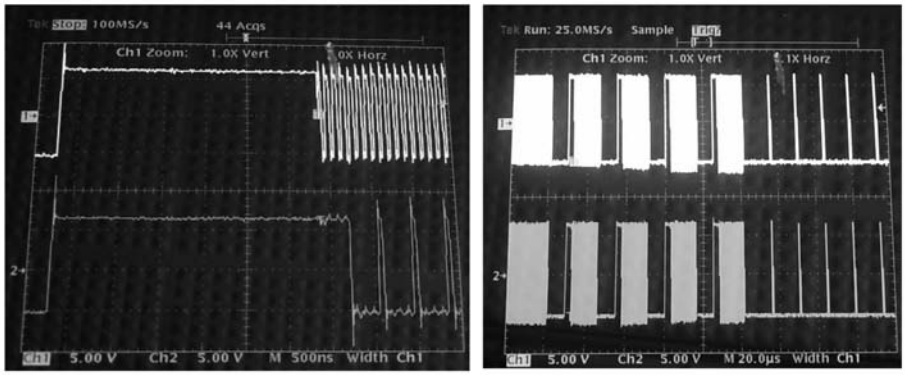


Fig. 3. Diagram of a very high frame rate camera based on an e2v CCD60.



(a) (b)

Fig. 4. The tested timing sequence of the imaging and storage area on the CCD.

In the designed CCD camera, the pixel rate is set at a maximum of 10 MHz, so the time to transfer the whole 128 rows of the charge in the image area to the storage area is simply computed as 128×100 ns=12.8 μs. After one frame, charges of the image area are transferred to the storage area, and so the image area is ready to catch another exposure; the integration time is set at about 12.2 μs. So the whole image acquisition frequency should be about 1/(12.8 μs+12.2 μs)=40000 Hz. The image readout rate is about
1/[(12.8 μs+12.2 μs)×4+134×142×100 ns]≈500 Hz.

4 Experiment and results

A prototype experiment has been carried out to test the time resolving ability of the newly designed camera. A xenon flash lamp is used as the timely changing light source, a PIN detector is used to monitor the light event, and a comparable 600fps camera [10] is used to capture the whole integration time image of the flash. Four images are acquired.

Figure 5(a) shows the trigger pulse exerted on the camera (ch1) and the xenon flash light attenuation curve (ch2). Fig. 5(b) shows the integrated image acquired by using the 600 fps camera. Fig. 5 (c1) to Fig. 5(c4) show the images acquired by the 40000 fps camera designed in this paper. It is clear that the newly designed CCD camera can acquire the developing sequence images of the xenon flash light. In the experiment, the start of image acquisition was arranged on the falling curve of the light (after the

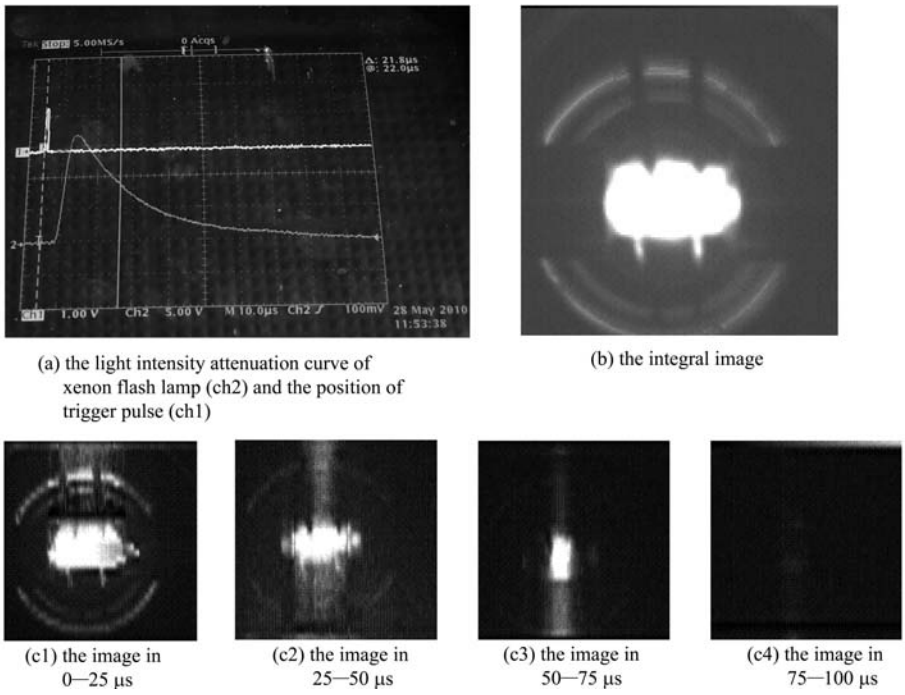


Fig. 5. The trigger timing and the images acquired by the very high frame rate camera.

delay of the trigger circuit of the CCD camera). The light intensity of the image sequence is decreasing.

5 Discussion

The innovative CCD driving method is mainly used on frame transfer CCDs to improve the image acquisition speed of the CCDs. The method provides the advantages of very high frame rate, sothere is no need for the peripheral memory to store the burst images, normal field of view, and a flexible vertical resolution for different applications. From the above description and the high frame rate camera implementation and the performance test on e2v CCD60, we can see that the method is effective in increasing the frame rate of the image acquisition. However, we must admit that the method also suffers some disadvantages. The first defect is that the ratio of transfer time to integration time is increased, which may cause a significant problem of smearing (Fig. 5(c1)–Fig. 5(c4)). The second defect is that the improvement of the frame rate is limited in only the image acquisition part, though the image readout rate remains. So in those cases where the fast read out speed is needed, the method is not a suitable solution. Of course, the resolution is also sacrificed as the driving method is combined with the CCD vertical binning.

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