Design and optimization of the readout system for X-ray CCDs*

LU Bo(陆波)[1)] CUI Wei-Wei(崔苇苇) WANG Yu-Sa(王于仨) ZHU Yue(朱玥)
ZHANG Yi(张艺) XU Yu-Peng(徐玉朋) CHEN Yong(陈勇) HUO Jia(霍嘉)
LI Wei(李炜) HAN Da-Wei(韩大炜) LI Mao-Shun(李茂顺) YANG Yan-Ji(杨彦佶)
WANG Juan(王娟) CHEN Tian-Xiang(陈田祥) HU Wei(胡渭)
LI Cheng-Kui(李承奎) LIU Xiao-Yan(刘晓艳)

Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China

Abstract: A readout system for X-ray CCDs based on an improved architecture is presented; by optimizing several critical circuit blocks along the analog signal chain, the conflict between the readout speed and readout noise is greatly alleviated. Using CCD47-10 as its target CCD, the readout system has achieved 8.6e$^-$ readout noise and 142 eV FWHM at 5.9 keV Mn K_α under a pixel rate of 80 kHz. Also its performance of imaging has been investigated.

Key words: CCD, X-ray, readout system

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1 Introduction

X-ray CCDs have been successfully employed as focal plane detectors of X-ray astronomical satellites such as ASCA, Chandra, XMM-Newton and SUZAKU, not only for their excellent spatial resolution but also their moderated energy resolution [1]. X-ray CCDs on board the satellites enable us to perform imaging and spectroscopy simultaneously in the soft X-ray band. Also, in the realm of detection of high-energy particles, such as dark matter, X-ray CCDs are emerging as a promising candidate.

Among the various performance parameters for X-ray CCDs, the time resolution and energy resolution are the two most important parameters for such applications as previously mentioned. The former is critical to distinguish the time-based events, while the latter, as is known to all, is directly related to spectrum quality. A modern X-ray CCD has active pixels at a typical order of 1M to help enlarge the field of vision, however, in high pixel-rate condition, it suffers a lot from the clock-induced noise generated by the CCD itself and its readout circuitry. For example, FWHMs at 5.9 keV Mn K_α from most of the similar systems are hardly below 150 eV with typical 50 kHz pixel rate [2, 3].

Many methods have emerged to solve these conflicting issues, including binning, region of interest, parallel readout and even dedicated ASICs [2]. Compared with the conventional method, they are either performance sacrificing or cost consuming. In this work, we present a readout system architecture with the back-illuminated CCD47-10 [4] from e2v as its target X-ray CCD. By optimization of such critical circuit blocks as the pre-amplifier (Pre-AMP), correlated doubling sampling (CDS), reference voltage generator (REF-GEN), baseline restoration circuit (BLR), threshold comparator (COMP), analog-to-digital converter (ADC), etc., we have achieved a good compromise between the readout speed and readout noise.

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1) E-mail: lubo@ihep.ac.cn

2 Architecture for readout system

The architecture of the readout system, shown in Fig. 1(a), consists of five main parts: the target CCD is used to generate the CCD signal; analog front-end (AFE) functions to abstract the effective signal and convert it to digital bitstream, including such analog components as Pre-AMP, CDS, COMP, REF-GEN, BLR as well as ADC; the bitstream is further packaged and transmitted through a USB cable to a PC by the control and transmission part, which is mainly made up of an FPGA and USB transmitter. The driving clocks required by the CCD are initially generated by FPGA and further tuned and buffered by the driver. The power supply provides the voltage biasings needed all over the system. Fig. 1(b) shows a photo of the practical system.

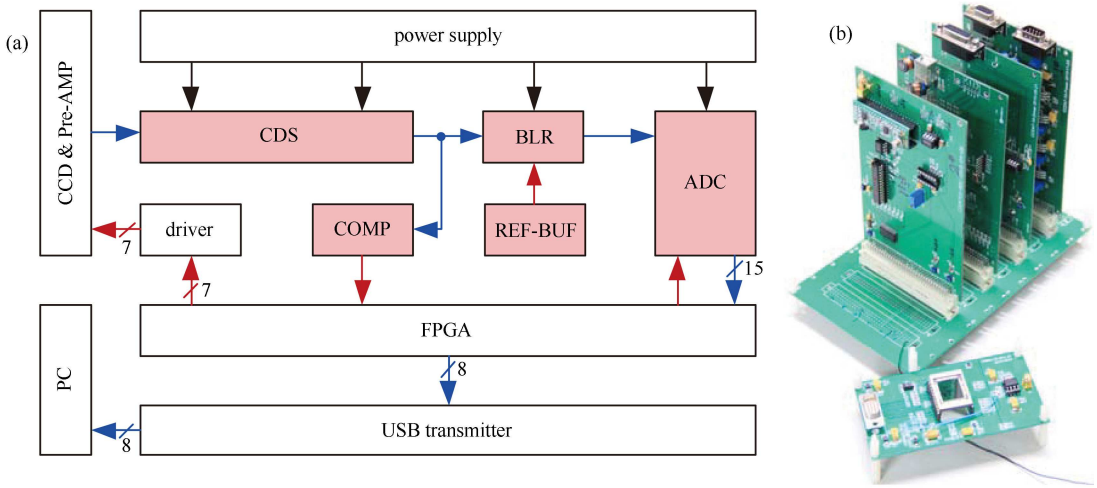

Fig. 1. The system architecture.

The characteristics of the presented architecture come from the following four aspects:

a)The CDS circuit is simplified, taking the sampling network of ADC as its actual-signal sampling part;

b)A simple and efficient BLR circuit is presented to cancel the voltage offset induced by the intrinsic thermal noise of the CCD itself;

c)A tuneable REF-GEN is adopted for signal polarity change and dynamic range adjustment to ease the signal chain design and efficiently use the dynamic range of ADC;

d)A COMP is introduced to adjust the data rate under the conditions of different X-ray sources.

Some of these characteristics will be covered in the next section.

3 Circuit design and optimization

3.1 CCD signal and ADC

A typical X-ray CCD signal and the presented timing scheme for AFE signal processing is shown in Fig. 2, where V_{D} is the intrinsic thermal noise of the CCD, which varies slightly pixel by pixel. V_{S} and V_{AS} are the integral signal and actual signal, respectively. Since our system is mainly engaged in the X-ray band under 25 keV, given the conversion ratio of CCD47-10 as 4.5 μV/e$^-$, the maximum actual signal level is calculated as 30.8 mV [5].

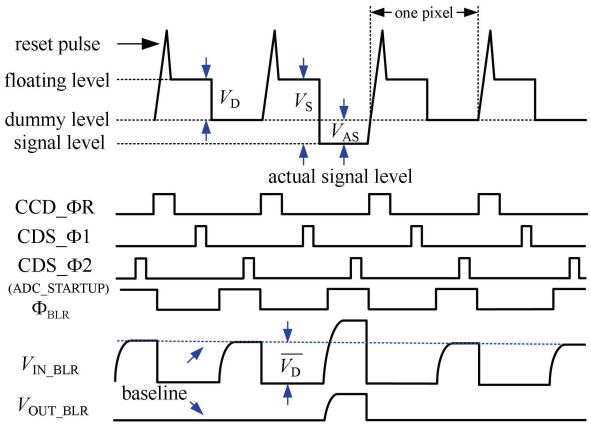

Fig. 2. System architecture.

ADC is chosen such that it can identify a single electron, resulting in a dynamic range from 3.65 eV to 25 keV, that means it requires at least 13 effective numbers of bits. In order to maintain enough margin of design, as well as alleviate the requirement for

the components along the signal chain, a 15-bit ADC AD976A [6] with a 20 V input voltage swing is used. The overall gain of the signal chain is thus tuned at about 220 V/V.

3.2 Pre-AMP circuit

The pre-AMP is the first circuit block that receives the CCD signal; noise from this circuit should not deteriorate the weak CCD signal, also, it should exhibit a low-pass characteristic to filter out the high frequency noise.

A low-noise TLE2072 [7] is competent for this purpose, the circuit is shown in Fig. 3. OP_1 is configured as a low-pass filter with its DC gain set to 10, the bandwidth is controlled by C_1 and R_2, which is optimized at almost 30 times the pixel rate. OP_2 is a unit-gain amplifier, giving enough driving capacity for the following circuits.

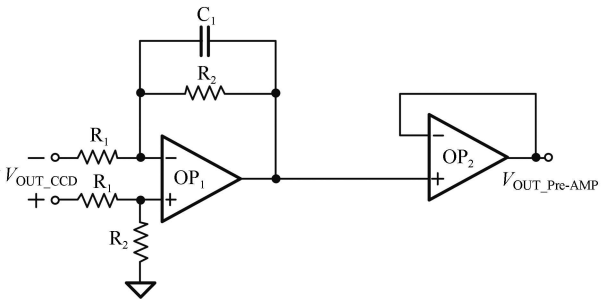

Fig. 3. Schematic of Pre-AMP.

3.3 CDS circuit

Since its debut on the stage of CCD signal processing, the sophisticated CDS technique has been dedicating itself to solving the intractable though common problems in X-ray CCD, such as removing the switching transients, eliminating the KT/C [8] noise associated with the combination of the reset switch and the related parasitic capacitors, and suppressing $1/f$ surface-state noise contribution. Typically, there is a pair of switch-capacitors in the CDS circuit, one is for instantaneous noise storage and cancellation, the other is for actual signal sampling, as shown in Fig. 4.

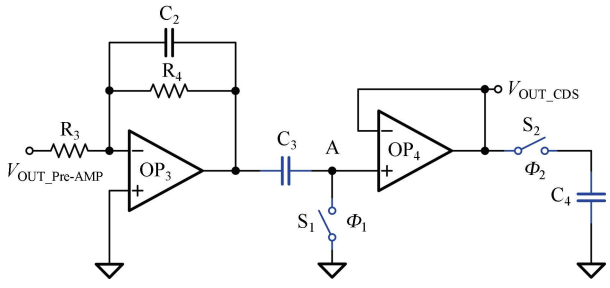

Fig. 4. Schematic of CDS.

The clamping switch S_1 is turned on when Φ_1 is high, and the noise from the proceeding circuitry is stored in C_3 and the output signal $V_{\rm OUT\_CDS}$ is pulled to ground. During the sampling phase Φ_2, S_2 and C_4 samples the actual signal. Provided the average intrinsic thermal noise is $\overline{V_{\rm D}}$ which could be soundly abtained by BLR circuit, the actual signal is calculated as

$$V_{\rm AS} = V_{\rm S} - \overline{V_{\rm D}}\,. \tag{1}$$

The time interval between the two clock phases has a critical effect on the lower frequency of the passband, so it is optimized such that the majority of the low-frequency noise is filtered out [5].

3.4 BLR circuit

The fact that the intrinsic thermal noise $V_{\rm D}$ varies pixel by pixel due to the thermal nature of dark current even under the same temperature, calls for an averaging process to eliminate the random noise. Despite its simplicity, an efficient BLR circuit is presented in Fig. 5.

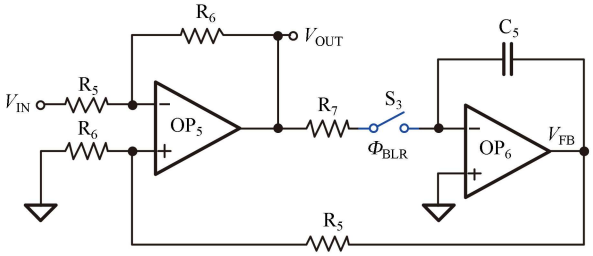

Fig. 5. Schematic of BLR.

It has a negative feedback configuration, S_3 is active only during the actual signal period as shown in Fig. 2; when $V_{\rm IN}$ exceeds $V_{\rm FB}$, the current through R_7 discharges C_5 in the integrator OP_6, making $V_{\rm FB}$ increase, and vice versa. The charging and discharging processes will not end until $V_{\rm FB}$ equals $V_{\rm IN}$. Through this mechanism, the average of $V_{\rm D}$ can be reached after several pixel periods in the presence of intrinsic thermal noise only. This circuit is particularly suitable for the photon-counting mode since the signal pixel only occupies a small portion of the total pixels.

4 Experiments and results

4.1 Experimental setup

We have conducted both X-ray spectrometry and imaging experiments to verify the performances of the presented readout system. Now that low temperature is a necessity for the suppression of dark

current noise, a vacuum tank is used, which is constructed by stainless steel with a thickness of 6 mm in order to keep out the natural space radiations. Before refrigeration by liquid nitrogen, the tank should first be vacuumized below 10^{-4} Pa by a molecular pump set. The CCD along with Pre-AMP is located inside the vacuum tank, while the rest of the readout system is set outside. The two separated parts are connected by SMA cable and several twisted-pair wires.

4.2 X-ray spectrometry

4.2.1 Spectrum of ^{55}Fe

For measurements of the readout noise and spectral resolution, a 1 μCi ^{55}Fe X-ray source is adopted to irradiate the target CCD, under the condition of 197 K temperature and 80 kHz pixel rate. In order to investigate the negative effect that charge transfer inefficiency (CTI) brings along, we have compared the FWHMs of the four different areas of the target CCD which are derived from the Gaussian fittings of the dominant peaks. The first three have the same pixel areas but with different distances from the output port, and the rest has the whole area, see Fig. 6, where the energy per channel is approximately 1.9 eV.

It seems that FWHM increases as the area becomes further away from the output port. We have confirmed from Fig. 6 that the CTI values are not uniform over the device.

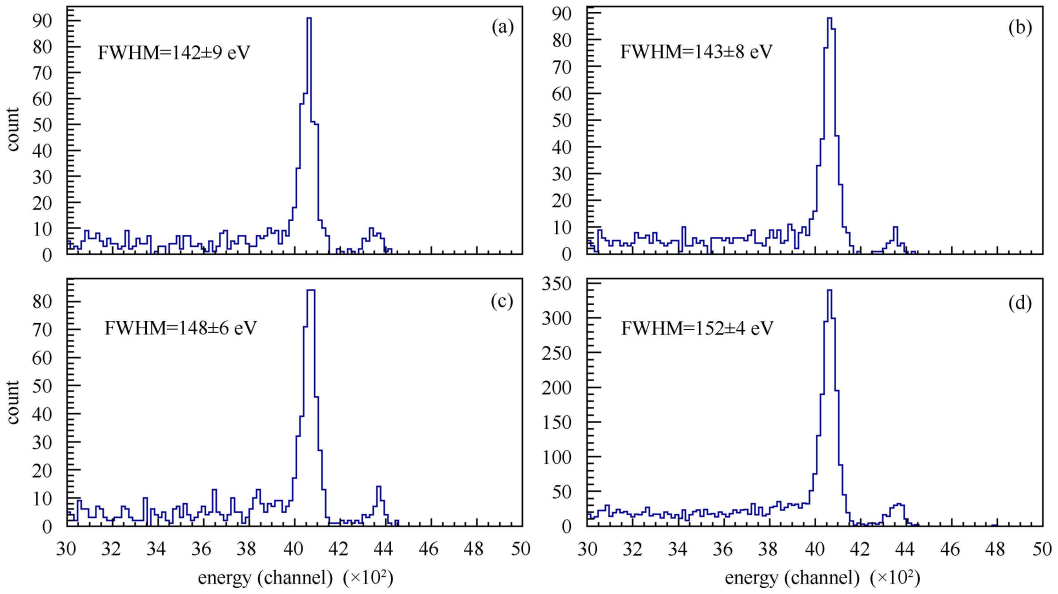

Fig. 6. ^{55}Fe spectrum obtained with (a) the nearest area; (b) the central area; (c) the furthest area; (d) the whole area.

4.2.2 Noise performance

An 8.6e$^-$ readout noise is directly obtained from the noise peak under the condition mentioned above, which is mainly made up of three parts including CCD intrinsic noise, back-end circuit noise and clock-induced noise. We have soundly found that the back-end circuit contributed most of the readout noise, which is approximately 5.4e$^-$ compared with 2.5e$^-$ generated by the CCD itself [5]. This result is commensurate with the widely-recognized conclusion that in the case of low-light conditions, the back-end circuit noise always dominates.

4.2.3 Spectrum of X-tube fluorescence

Generally, a variety of fluorescences can be generated when X-rays from the X-tube bombard the stainless steel, amid which the Al K_α, Cr K_α, Fe K_α, and W L_α peaks are expected to be prominent. This fact gives a promising way to investigate the linearity of the readout system as well as the split-event phenomenon. Fig. 7 gives the spectrum and corresponding fitting result.

4.3 Imaging

Both the visible-light imaging and scintillator

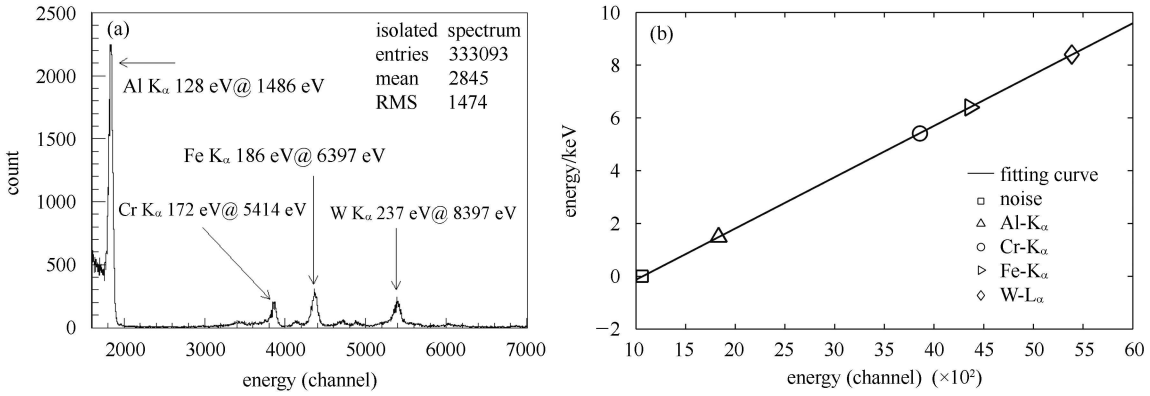

Fig. 7. X-tube fluorescence: (a) spectrum; (b) fitting curve.

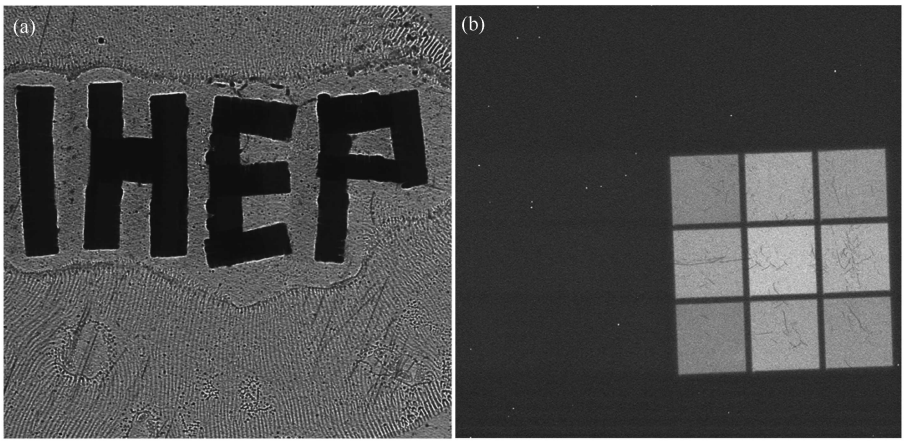

Fig. 8. Imaging with: (a) visible light @room temp.; (b) ^{241}Am and CsI(Tl) @230 K.

imaging have been conducted to investigate the imaging performance of the presented readout system. The exposure time is 1ms using LED light for the former, while 100s using ^{241}Am for the latter. Both of them have a frame rate of 0.115 Hz. The corresponding images are shown in Fig. 8.

5 Conclusions

We have developed a readout system for X-ray CCDs using discrete components. By optimizing the system architecture, and several critical analog circuit blocks as well, most of the clock-induced noise is eliminated even under a considerable high pixel rate. Noise and speed are actually a pair of intractable issues in the readout system design for every CCD, which requires tradeoffs not only in circuit design but also in PCB layout design. Although we have not yet illustrated the impact of PCB layout in this paper, its importance should never be overlooked in practical design.

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