Clock auto-synchronization method for BESIII ETOF upgrade*

WANG Si-Yu(王思宇)[1,2] CAO Ping(曹平)[1,2;1)] LIU Shu-Bin(刘树彬)[1,2] AN Qi(安琪)[1,2]

[1] State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China
[2] Anhui Key Laboratory of Physical Electronics, Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China

Abstract: An automatic clock synchronization method implemented in a field programmable gate array (FPGA) is proposed in this paper. It is developed for the clock system which will be applied in the end-cap time of flight (ETOF) upgrade of the Beijing Spectrometer (BESIII). In this design, an FPGA is used to automatically monitor the synchronization circuit and deal with signals coming from the external clock synchronization circuit. By testing different delay time of the detection signal and analyzing the signal state returned, the synchronization windows can be found automatically by the FPGA. The new clock system not only retains low clock jitter which is less than 20ps root mean square (RMS), but also demonstrates automatic synchronization to the beam bunches. So far, the clock auto-synchronizing function has been working successfully under a series of tests. It will greatly simplify the system initialization and maintenance in the future.

Key words: BESIII, endcap time-of-flight, clock synchronization

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1 Introduction

The Beijing Electron Positron Collider (BEPC) and the Beijing Spectrometer (BES) [1, 2] were upgraded to BEPCII and BESIII [3–5] respectively in the summer of 2008. The time-of-flight (TOF) system, with the physics goal of particle identification (PID), is a very important part of BESIII. To improve the time resolution of the PID, the newly developed and widely used gaseous detector, multi-gap resistive plate chamber (MRPC) [6–8], has been chosen for an upgrade of the end-cap TOF (ETOF) detector instead of plastic scintillator bars read out by fast fine mesh photomultiplier tubes (PMTs). After upgrade, the total time resolution will be improved significantly from 138 ps in total to better than 80 ps, of which the limitation caused by electronics should be 25 ps or less [9].

To ensure the 25 ps time resolution of the TOF electronics, the clock jitter must be less than 20 ps RMS and the clock phase should be highly synchronized to the beam collision time [10]. As MRPC detectors are utilized in the upgrade system, there is a significant increase in the number of electronics channels and two more VME64xP crates as well as another two clock modules will be needed for dedicated use by the ETOF electronics system [11]. Thus, to meet the needs of the upgraded system, more clock output channels need to be added to the original clock system. On the other hand, each time the original TOF system is powered on it requires a series of manual operations to configure the clock synchronization which is not very intelligent. As the TOF clock system is under upgrade, the configuration operations will be simplified with the help of a new algorithm implemented in a field programmable gate array (FPGA).

2 Automatic clock synchronization method

2.1 Proposed clock system

To meet the needs of the TOF electronics, the proposed clock system consists of two parts: one for transmission of the RF signal, and the other composed of VME clock modules which are responsible for providing multi-channel high quality clocks as well as synchronization and phase-control between them.

Figure 1 is a block diagram of the whole TOF clock system. The accelerator provides the RF clock signal which is transmitted by optical fiber. To minimize the effects of temperature change, the optical transmitters and receivers from the Ortel company and Phase-Stabilized

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1) E-mail: cping@ustc.edu.cn

Optical Fiber (PSOF) from the Furukawa company are used. The RF clock signal is transmitted to the VME clock modules for clock generation and fan-out.

Considering the structure of the TOF read-out system before upgrade, a master-slave mode is still used in this new clock system. It now contains four clock modules: one is a master module and the others are slave modules. In addition, the master module is also required to be able to generate clocks and synchronize them for the whole TOF read-out electronics system. To simplify the design, both master and slave clock modules share the same circuit design, of which the scheme is shown in Fig. 2.

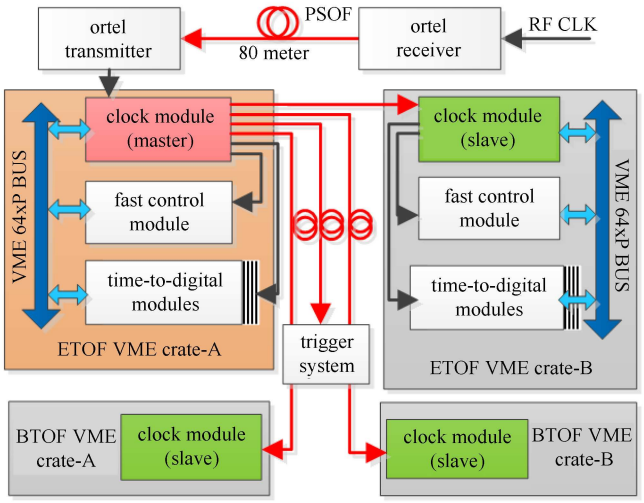

Fig. 1. (color online) Block diagram of TOF clock system.

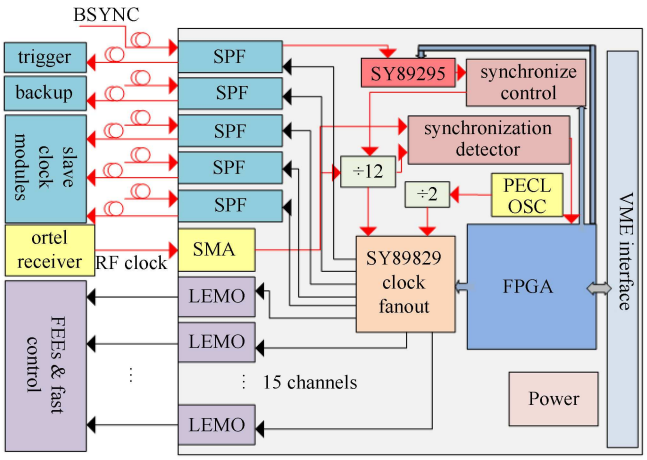

Fig. 2. (color online) Scheme of the clock module.

By selecting different clock sources for the clock fan-out chip, the clock module will work under master or slave mode. In master mode, the system clock is the 499.8 MHz RF clock from the accelerator, divided by 12; in slave mode, it is a 41.67 MHz optical signal output from the master clock module. Besides, every clock module has an 83.3 MHz crystal oscillator onboard for clock generation by itself under off-line mode. The clock fan-out chip SY89829 has a 20-channel output, of which five channels are transformed to optical signals for the trigger systems and slave modules, and the other fifteen channels are transmitted in the form of LVPECL electrical signals to other VME modules which are located in the same VME64xP crate.

An FPGA is also used for system control. It supports communication between the computer and electronics system via VME interface protocol.

2.2 Clock synchronization and monitoring

The period of beam bunches in the accelerator is 8 ns and the synchronized RF signal is 499.8 MHz. As mentioned before, the TOF clock is generated by a simple divider so that there are four possible phases between the beam bunches and the TOF clock. To get a constant phase for the TOF clock, a BSYNC signal is derived from the accelerator for phase adjustment of which the leading edge contains the phase information of the beam bunches. Therefore, clock synchronization will be achieved once the time interval between the leading edge of BSYNC and that of the TOF clock is determined. A simplified diagram of the synchronization control and clock generation circuit design is shown in Fig. 3 [10].

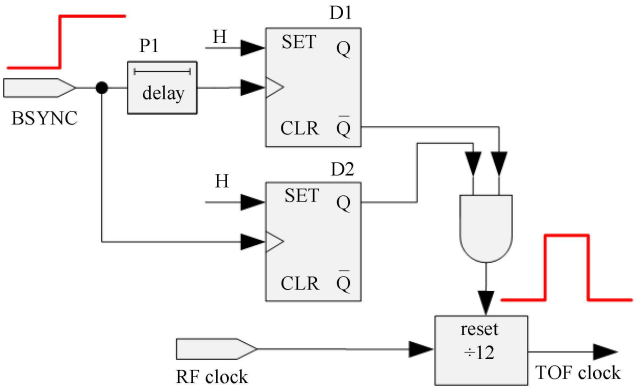

Fig. 3. (color online) Simplified diagram of synchronization control and clock generation circuit.

A periodic clock signal is formed by two D-flip-flops (DFFs) which convert the TOF clock duty from 1/2 to 1/12. This new signal has the same phase as the TOF clock so it can be used to check the current clock synchronization state, as shown in Fig. 4 [10].

Once the clock phase is determined, we can get a synchronization window by adjusting the delay value of the BSYNC signal. Theoretically the window width should be 2 ns, but considering the instability of the edge of signals output from the DFFs, the actual window width

will be slightly less than 2 ns. Corresponding to the different phases of the TOF clock, there is more than one synchronization window, and all of them are connected one-by-one to the delay-time axis. However, the final synchronization window that we choose is determined by the desired phase of the TOF clock.

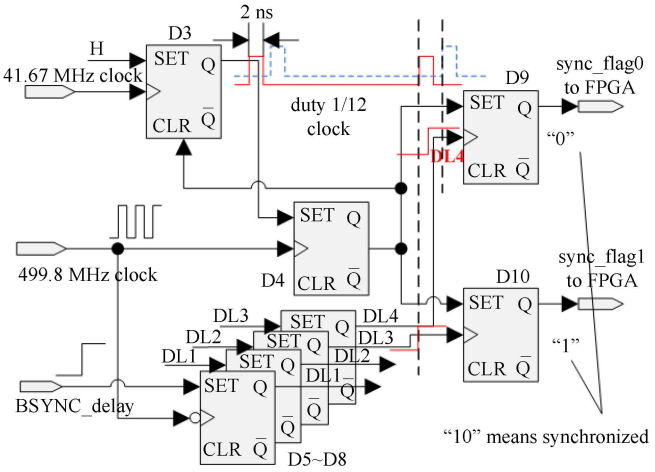

Fig. 4. (color online) Simplified diagram of synchronization monitor circuit.

2.3 Algorithm in FPGA

In the previous TOF clock system, a lot of VME read and write operations to measure the synchronization windows and calculate the center value had to be done manually. Even a small change in the system, for instance, a replacement of transmission cables, requires the synchronization windows to be re-measured. To simplify the synchronization operation, a method of automatic clock synchronization has been implemented in the FPGA.

As mentioned above, the BSYNC signal is delayed by a SY89295 chip [12]. The chip is a programmable delay line that delays the input signal using a 10-bit-long digital control signal. The delay can vary from 3.2 ns to 14.8 ns in 10 ps increments. Then, the synchronization state will be adjustable by changing different configuration data from the FPGA to the delay chip. The automatic synchronization starts with a reset signal of dividers according to an initial delay data. If the feedback synchronization flag (SynFlag) is '10', then the following operations can be continued; otherwise, the initial delay data should be slightly increased in value to make the system work in a steady state of some specific synchronization window.

Figure 5 shows a flowchart for the automatic synchronization logic, which mainly consists of two parts - Step 1 and Step 2. Their purpose is to measure the maximum and minimum values of synchronization window respectively. By changing the delay value from coarse count to fine count and testing whether the value of SynFlag is '10', the boundary values of the synchronization interval will be found. Finally, the center value can be easily calculated by averaging the boundary values, and this can then be used as the delay value for synchronization calibration that makes sure the whole TOF system works under the same clock phase after powering on.

On both sides of the boundary of the synchronization window, there is a short unstable interval and whether it is actually in the range of synchronization window cannot be determined by just a single measurement. Thus, during measurement of the maximum and minimum values, the result will be considered correct only if the synchronization flag obtained is "10" more than 8 times. Figure 6 shows a schematic of the TOF clock synchronization window.

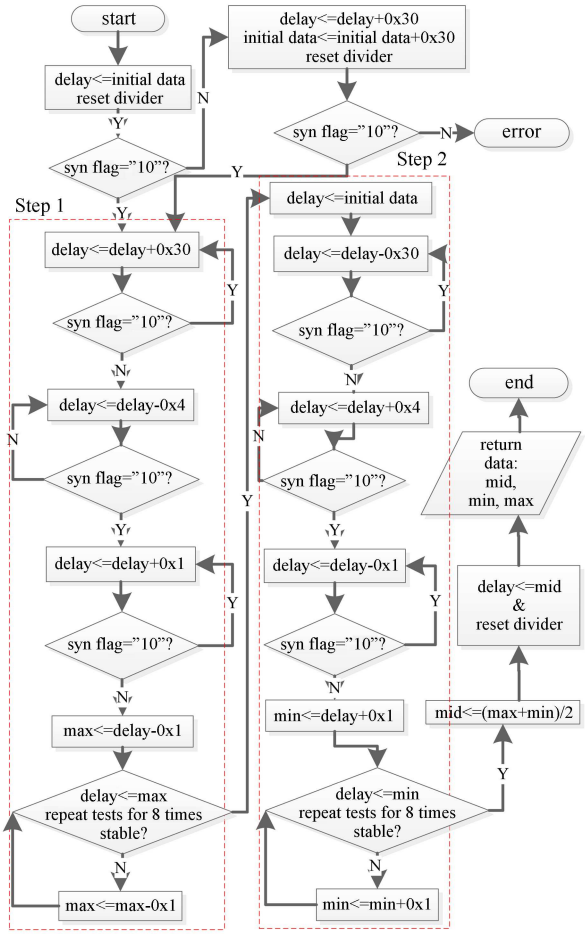

Fig. 5. (color online) Logic flowchart of automatic synchronization.

This procedure can be called to control the TOF clock synchronization every time after system power-on. While power is on, this logic module can also be called to re-measure the synchronization window automatically by

VME reading and writing. Meanwhile, the new logic can not only test the representative values of the synchronization window automatically, but also retains the manual operation and detection functions from the old TOF clock system, which means that we can get the information in both ways and verify the reliability of the results.

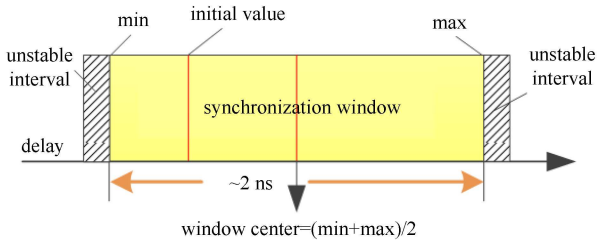

Fig. 6. (color online) Schematic of synchronization window.

At present, the clock system alarm is triggered by DAQ control when errors occur during synchronization detection. The DAQ reads the status register in clock module and generates alarm signals. A better way to achieve an alarm function for the clock system is to send error information to the fast-control module. The fast-control module will request interrupts and send an alarm to the system immediately.

3 Test results

For the new TOF clock module test, two optical fibers of different lengths were used to transmit the BSYNC signal in the TOF clock system. The synchronization information is shown in Table 1.

Table 1. Synchronization of different optical fibers.

register	function	delay using fiber A		delay using fiber B	
		(0xX)	(ps)	(0xX)	(ps)
0xf050	center	0x174	3348	0x11d	2565
0xf0c0	minimum	0x108	2376	0xb0	1584
0xf0d0	maximum	0x1e0	4320	0x18b	3555

There are significant differences in the positions of the two synchronization windows caused by the different initial phases between the BSYNC signal and the RF clock. One bit in the delay chip corresponds to approximately 9 ps so the actual delay values in the table are obtained by data in decimal format multiplied by 9 ps.

To get all the synchronization windows, different initial delay values were provided. As mentioned before, there are unstable intervals at the edges which may cause overlaps of adjacent windows. After improving the correction algorithm by measuring repeatedly near the edges of synchronization windows, the overlaps are all gone, as shown in Table 2.

When the synchronization configuration is done, the rising edge of the delayed BSYNC signal will decide the system clock phase. The specific waveform of the BSYNC_delay signal and 1/12 40 MHz Clock signal is illustrated in Fig. 7. The system clock has been demonstrated to be well synchronized to the beam bunches.

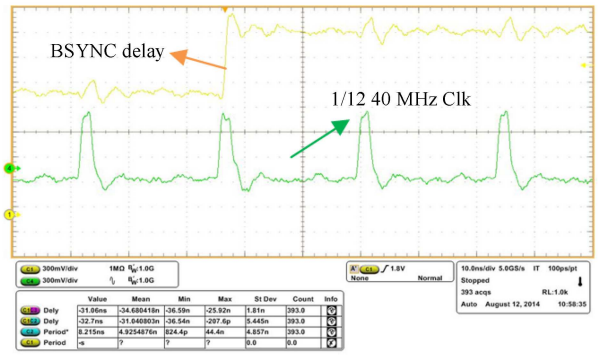

Fig. 7. (color online) Waveform of synchronized clock and BSYNC_delay.

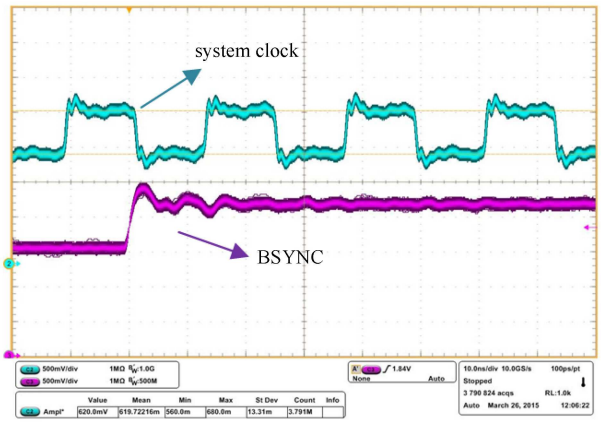

Fig. 8. (color online) Waveform of synchronized clock and BSYNC with infinite persistence turned on.

Table 2. Detection of synchronization windows.

register	function	before correction			after correction		
		window1	window2	window3	window1	window2	window3
0xf040	initial	0x100	0x1c0	0x290	0x100	0x1a0	0x280
0xf050	center	0x11d	0x1fc	0x2d5	0x10d	0x1e3	0x2b9
0xf0c0	minimum	0xb0	0x18c	0x268	0xa4	0x178	0x250
0xf0d0	maximum	0x18b	0x26c	0x343	0x177	0x24e	0x322

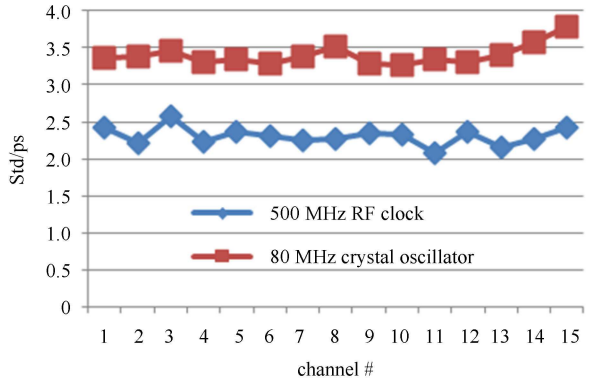

Fig. 9. (color online) Jitter performance for clock modules.

To verify the stability of this auto-synchronization method, the phase between the system clock and BSYNC signal has been checked by a Tektronix DPO5104 oscilloscope with infinite persistence turned on. The waveform is shown in Fig. 8. This test result shows that there is no uncertainty between these two signals.

Since there is almost no change in the clock module circuit, the system clock jitter remains less than 20 ps RMS. This has already been reconfirmed by further tests. The measured period jitter (standard deviation) for clock channels are shown in Fig. 9.

4 Conclusions

In this paper, a method of automatic clock synchronization implemented in FPGA is proposed for the clock system of the BESIII ETOF upgrade. It combines both FPGA algorithm and external off-the shelf devices. The synchronization intervals can be calculated automatically by adjusting the external delay chip and analyzing the returned synchronization flags. According to test results, the function of automatic clock synchronization to the beam collision time has been achieved without any adverse influences on the system clock quality.

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